Publications

Book contributions

1. K. L. Shepard and V. Narayanan, "Harmony: A methodology for noise analysis in deep submicron digital integrated circuits," reprinted in *Signal Integrity Effects in Custom IC and ASIC Design*, Raminderpal Singh, editor, IEEE Press, 2002.
2. K. L. Shepard and D.-J. Kim, "Static noise analysis for digital integrated circuits in partially-depleted silicon-on-insulator technology," reprinted in *Signal Integrity Effects in Custom IC and ASIC Design*, Raminderpal Singh, editor, IEEE Press, 2002.
3. M. L. Roukes, *K. L. Shepard*, and B. P. Van der Gaag, "Electron scattering experiments in mesoscopic conductors," in Science and Technology of Mesoscopic Structures, Springer-Verlag, 1991.

Journal/Magazine Publications

1. Y. Zheng and *K. L. Shepard*, "On-chip oscilloscopes for noninvasive time-domain measurement of waveforms in digital integrated circuits," IEEE Transactions on VLSI, June, 2003, pp. 336-344.

2. Steven C. Chan, *K. L. Shepard*, and Dae-Jin Kim, "Static noise analysis for digital integrated circuits in partially depleted silicon-on-insulator technology," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, August, 2002, pages 916-927.

3. *K. L. Shepard* and D.-J. Kim, ``Body-voltage estimation in digital PD-SOI circuits and its application to static timing analysis," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, July, 2001, pages 888-901.

4. *K. L. Shepard* and Z. Tian, ``Return-limited inductance: A practical approach to on-chip inductance extraction," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, April, 2000, pages 425-436.

5. *K. L. Shepard*, V. Narayanan, and R. Rose, ``Harmony: A methodology for noise analysis in deep submicron digital integrated circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, August, 1999, pages 1132 - 1150.

6. *K. Shepard*, ``A Headache on Top of a Migraine: The Challenge of SOI," Integrated Systems Design Electronics Journal, December, 1998, pages 14-15.

7. *K. L. Shepard* and V. Narayanan, "Conquering noise in deep submicron digital ICs," IEEE Design and Test of Computers, January-March, 1998

8. *K. L. Shepard*, S. M Carey, E. K. Cho, B. W. Burran, R. F. Hatch, D. E. Hoffman, S. A. McCabe, G. A. Northrop, and R. Seigler, "Design methodology for the S/390 Parallel Enterprise Server G4 microprocessors," IBM Journal of Research and Development, Volume 41, Number

4/5, pages 515-547, July/September, 1997

9. C. F. Webb, C. J. Anderson, L. Sigal, *K. L. Shepard*, J. S. Liptay, J. D. Warnock, B. Curran, B. W. Krumm, M. D. Mayo, P. J. Camporese, E. M. Schwarz, M. S. Farrell, P. J. Restle, R. M. Averill III, T. J. Slegel, W. V. Huott, Y. H. Chan, B. Wile, T. N. Nguyen, P. G. Emma, D. K. Beece, C.-T. Chuang, and C. Price, "A 400-MHz S/390 microprocessor," IEEE Journal of Solid-State Circuits, November, 1997, pages 1665-1675.

10. *K. L. Shepard*, M. L. Roukes, and B. P. van der Gaag, "Experimental measurement of scattering coefficients in mesoscopic conductors," Physical Review B 46, 9648 (1992)

11. *K. L. Shepard*, M. L. Roukes, and B. P. van der Gaag, "Direct measurment of the transmission matrix of a mesoscopic conductor," Phys. Rev. Lett 68, 2660 (1992)

12. *K. L. Shepard*, "Antiscreening and exchange-enhanced spin-splitting in quantum wires," Physical Review B 45, 13431 (1992)

13. *K. L. Shepard*, "Disorder and the transition to the quantum Hall regime in quasi-one-dimensional channels," Physical Review B 44, 9088 (1991)

14. *K. L. Shepard*, "Multichannel, multiprobe Landauer formula in the presense of a uniform magnetic field," Physical Review B 43, 11623 (1991)

15. *K. Shepard* and H. Schumacher, "Scaling in Npn and Pnp heterostructure bipolar transistors," Electronics Letters 24, 111 (1988)

16. *K. Shepard*, Z E. Smith, S. Aljishi, and S. Wagner, "Kinetics of the generation and annealing of deep defects and recombination centers in amorphous silicon," Applied Physics Letters 53, 1644 (1988)

17. Z E. Smith, V. Chu, *K. Shepard*, S. Aljishi, D. Slobodin, J. Kolodzey, S. Wagner, and T. L. Chu, "Photothermal and photoconductive determination of surface and buld defect densities in amorphous silicon films," Applied Physics Letters 50, 1521 (1987)

Conference Publications

1. S. Rajapandian, Z. Xu, and K. L. Shepard, "Charge-recycling voltage domains for energy-efficient low-voltage operation of digital CMOS circuits," Proceedings of the 2003 International Conference on Computer Design (to appear)

2. S. C. Chan, K. L. Shepard, and P. J. Restle, "Design of resonant global clock distributions," Proceedings of the 2003 International Conference on Computer Design (to appear)

3. Y. Li, G. Patounakis, K. L. Shepard, "High-throughput asynchronous datapath with software-controlled voltage scaling, " VLSI Circuits Symposium, June, 2003.

4. Y. Li, G. Patounakis, A. Jose, K. L. Shepard and S. M. Nowick, "Asynchronous datapath with software-controlled on-chip adaptive voltage scaling for multirate signal processing

applications, " Proceedings of the International Symposium on Asynchronous Circuits and Systems, May, 2003.

5. Dipak Sitaram, Yu Zheng, and K. L. Shepard, "Implicit treatment of substrate and power-ground losses in return-limited inductance extraction," Proceedings of the International Conference on Computer-Aided Design, 2002.

6. Steven Chan and *K. L. Shepard*, ``Practical considerations in RLCK crosstalk analysis for digital integrated circuits," Proceedings of the International Conference on Computer-Aided Design, 2001, pages 598-604.

7. *K. L. Shepard* and Yu Zheng, ``On-chip oscilloscopes for noninvasive time-domain measurement of waveforms," Proceedings of the International Conference on Computer Design, September, 2001, pp. 221-226. *Best paper award winner*

8. *K. L. Shepard*, ``CAD Issues for CMOS VLSI Design in SOI," Proceedings of the International Symposium on Quality in Electronic Design, March, 2001, pages 105-110 (*invited*)

9. *K. L. Shepard*, D. Sitaram, and Y. Zheng, ``Full-chip, shapes-based RLC extraction," Proceedings of the International Conference on Computer-Aided Design, November, 2000, pages 142-149.

10. *K. L. Shepard* and D.-J. Kim, ``Static noise analysis for digital integrated circuits in partially-depleted silicon-on-insulator technology," Proceedings of the Design Automation Conference, June, 2000, pages 239-242.

11. *K. L. Shepard* and K. Chou, ``Cell characterization for noise stability," Proceedings of the Custom Integrated Circuits Conference, 2000, pages 91-94.

12. *K. L. Shepard* and D.-J. Kim, ``Body-voltage estimation in digital PD-SOI circuits and its application to static timing analysis," Proceedings of the International Conference on Computer-Aided Design, 1999, pages 531-538

13. M. Kamon, S. McCormick, and *K. L. Shepard*, ``Interconnect Parasitic Extraction in the Digital IC Design Methodology," Proceedings of the International Conference on Computer-Aided Design, 1999, pages 223-230.

14. *K. L. Shepard* and Z. Tian, "Return-limited inductances: A Practical Approach to On-Chip Inductance Extraction", Proceedings of the 1999 Custom Integrated Circuits Conference.

15. *K. L. Shepard*, "The challenge of high-performance, deep-submicron design in a turnkey ASIC environment", Proceedings of the 1998 International ASIC conference, pp. 183-186. (*invited*)

16. *K. L. Shepard*, "Design methodologies for noise in digital integrated circuits," Proceedings of the Design Automation Conference, 1998.

17. R. Puri and *K. L. Shepard*, ``Timing issues in static-dynamic synthesis," ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, 1997.

18. C. F. Webb, C. J. Anderson, L. Sigal, *K. L. Shepard*, J. S. Liptay, J. D. Warnock, B. Curran, B.

W. Krumm, M. D. Mayo, P. J. Camporese, E. M. Schwarz, M .S. Farrell, P. J. Restle, R. M. Averill, III, T. J. Slegel, W. V. Huott, Y. H. Chan, B. Wile, and P. Emma, "A 400MHz S/390 Microprocessor," Proceedings of the International Solid-State Circuits Conference, 1997, pages 168-169.

19. *K. L. Shepard*, V. Narayanan, P. C. Elmendorf, and Gutuan Zheng, "Global Harmony: Coupled noise analysis for full-chip RC interconnect networks," Proceedings of the International Conference on Computer-Aided Design, 1997, pages 139-146

20. *K. L. Shepard*, S. Carey, D. K. Beece, R. Hatch, and G. Northrop, "Design Methodology for the High-Performance G4 3/390 Microprocessor," Proceedings of the International Conference on Computer Design, 1997, pages 232-240

21. *K. L. Shepard*, "Practical Issues of Interconnect Analysis in Deep Submicron Integrated Circuits," Proceedings of the International Conference on Computer Design, 1997, pages 532-541

22. *K. L. Shepard* and V. Narayanan, "Noise in deep submicron digital design," Proceedings of the International Conference on Computer-Aided Design, 1996, pages 524-531

Workshops/Tutorials

1. ``Tutorial: Modelling Technology for High Frequency Design ," Design Automation Conference, June, 2002.

2. ``Tutorial: Electrical integrity design and verification for digital and mixed-signal systems-on-a-chip," International Conference on Computer-Aided Design, November, 2001.

3. ``Tutorial: Interconnect-centric electrical integrity verification for systems-on-a-chip," International Conference on Computer-Aided Design, San Jose, November, 2000

4. `` Noise in CMOS VLSI Chips," Vail Computer Elements Workshop, June, 2000

5. ``Tutorial: Accurate analysis of crosstalk effects in VDSM designs," International Conference on Quality in Electronic Design, San Jose, March 2000.

6. ``Tutorial: Ultra Deep Submicron Design and Analysis," Asian-Pacific Design Automation Conference, Yokohama, Japan, February, 2000

7. ``Panel: How will CAD handle billion-transistor systems?" International Conference on Computer Aided Design, November, 1998.

8. ``Panel: Taming noise in deep submicron digital design," Design Automation Conference, San Francisco, CA, June, 1998

9. ``Tutorial: Analysis/optimization of performance and noise in deep submicron designs," Asian-Pacific Design Automation Conference, Yokohama, Japan, February, 1998

10. NSF workshop on systems-in-silicon, Princeton University, March, 1998

11. ``Technology and trends for static timing analysis in deep submicron digital integrated circuits," International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, Austin, December, 1997 (*invited*)

12. ``Timing in deep submicron digital design," Computer Elements Workshop, Mesa, Arizona, 1996